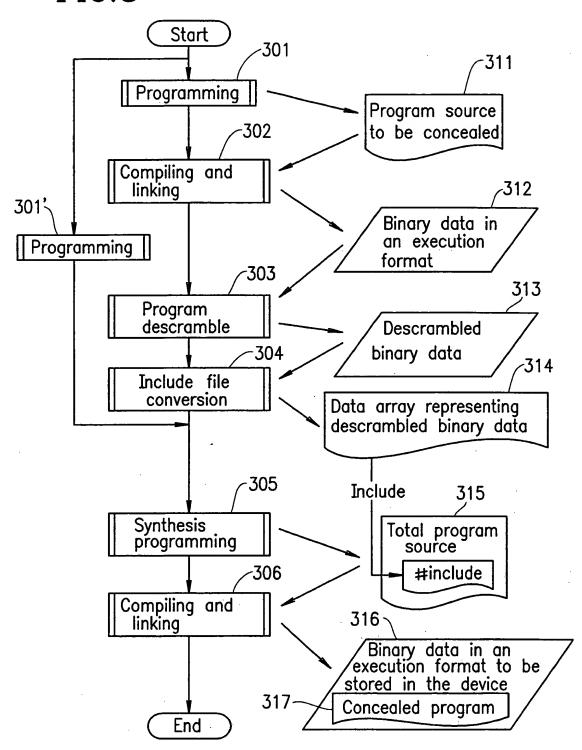
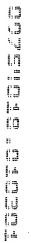


FIG.3





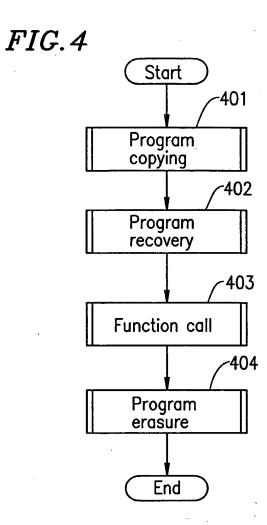


FIG.5A 100 106 -102 -103 Data scramble circuit Others circuits MPU ₁₀₇ Internal bus 500 502 317 500 Rewritable Program memory -105 -104 memory

